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| APPLICATION NO.   | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------|------------------|
| 10/017,342  | 12/13/2001  | Robert Hundt         | 10019982-1          | 6805             |
| 7590  | 05/20/2005  |                      | EXAMINER            |                  |
| HEWLETT-PACKARD COMPANY<br>Intellectual Property Administration<br>P.O. Box 272400<br>Fort Collins, CO 80527-2400 |             |                      | MITCHELL, JASON D   |                  |
|   |             |                      | ART UNIT            | PAPER NUMBER     |
|   |             |                      | 2193                |                  |

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| <b>Office Action Summary</b> | <b>Application No.</b> | <b>Applicant(s)</b> |
|------------------------------|------------------------|---------------------|
|                              | 10/017,342             | HUNDT ET AL.        |
| Examiner                     | Art Unit               |                     |
| Jason Mitchell               | 2193                   |                     |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

1)  Responsive to communication(s) filed on 23 February 2005.

2a)  This action is **FINAL**.                    2b)  This action is non-final.

3)  Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

4)  Claim(s) 1-15 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5)  Claim(s) \_\_\_\_\_ is/are allowed.

6)  Claim(s) 1-15 is/are rejected.

7)  Claim(s) \_\_\_\_\_ is/are objected to.

8)  Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

9)  The specification is objected to by the Examiner.

10)  The drawing(s) filed on 23 February 2005 is/are: a)  accepted or b)  objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)  The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a)  All b)  Some \* c)  None of:  
1.  Certified copies of the priority documents have been received.  
2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3.  Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)  Notice of References Cited (PTO-892)  
2)  Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3)  Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date . . . .  
4)  Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_ .  
5)  Notice of Informal Patent Application (PTO-152)  
6)  Other: . . . .

### DETAILED ACTION

1. This action is in response to an application filed on 12/13/01.
2. Claims 1-15 are pending in this case.
3. This action is **Non-Final** as a result of the new grounds of rejection.

### *Drawings*

4. Applicant's replacement drawings and amendments to the specification were sufficient to over come the objections to the drawings.

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. **Claims 1-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,189,141 to Benitez et al. (Benitez).**

**Regarding Claims 1, 6 and 11:** Benitez discloses reverting a process in an in-line instrumented state to an uninstrumented state (col. 4, lines 21-22 'removes a hot trace') by modifying selected text segment portions from said process (col. 29, lines 19-24 'a target address of a translated instruction ... is replaced with the address of the corresponding original instruction'); unmapping instrumented code space such that said instrumented code space is inaccessible to said process (col. 27, lines 49-51 'changes

hot block storage management map so that ... coldest blocks are indicated to be available'); provided an instruction pointer resides in said instrumented code space, updating said instruction pointer to uninstrumented code space (col. 29, lines 19-24 'address of a translated instruction ... is replaced with the address of the corresponding original instruction'); and executing said process and, provided said process generates a fault, providing a corresponding address in said uninstrumented code space (col. 11, lines 28-38 'an error condition has been detected ... control is returned to interrupter-presenter ... resuming conventional execution').

Benitez does not explicitly disclose that said process generates the fault by seeking to access an address in instrumented code space. However Benitez does teach that control should be returned to fetcher 430 when (col. 30, 'If cold trace detector and remover 1220 had not been invoked, ... time may be spent returning control to instruction fetcher 430'), and it would have been obvious to a person of ordinary skill in the art at the time of the invention to raise a fault (col. 11, lines 28-38 'an error condition has been detected') in this instance as a means of returning control to the uninstrumented code (col. 30, 'returning control to instruction fetcher 430').

**7. Claims 2, 7 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,189,141 B1 to Benitez et al. (Benitez).**

**Regarding Claims 2, 7 and 12:** The rejections of claims 1, 6 and 11 are incorporated respectively; further, Benitez discloses said selected text segment portions are selected from the group consisting of: branches, switch tables, procedure lookup tables (PLTs) for said instrumented code space (col. 29, line 20 'backpatches a jump'). Please note

that branches, switch tables and PLT's are all considered jumps (col. 2, lines 62-65 'transferring control over an arc ... is referred to as a jump').

Benitez does not explicitly disclose the text segment portions being selected from a group of breakpoints however he does disclose changing instructions that facilitate debugging and monitoring (col. 34, lines 16-20 'such functions as debugging, ... monitoring')

It would have been obvious to a person of ordinary skill in the art at the time of the invention to include text segment portions representing breakpoints in addition to the jump instructions explicitly disclosed in Benitez (col. 29, line 20) because one of ordinary skill in the art would want the ability to provide a more complete translation of the code (col. 34, lines 11- 16 'may instrument, or other wise translate, instructions ... in addition to such instrumentation').

**Regarding Claims 3, 8 and 13:** The rejections of claims 1, 6 and 11 are incorporated respectively; further, Benitez discloses said instrumented code space is comprised of shared memory (col. 10, lines 15-16 'instruments hot blocks and stores them in main memory').

**Regarding Claims 4, 9 and 14:** The rejections of claims 1, 6 and 11 are incorporated respectively; further, Benitez discloses unwinding a call stack of said process and recording return addresses of said process (Fig. 6D).

The hot block-arc table shown in Fig. 6D is a record of jumps the execution has followed. The value in column 222D represents the target address of each jump instruction (col. 28, line 3 'column 222D ... the jump arc target'), and the value of

column 222B represents the jump instruction's address (col. 28, lines 22-27 'the "starting hot block address" ... represented by column 212B'). The Backpatcher follows a path retrieved from this table (col. 2, lines 1-3 'determination is made by examining the fields for each record') in order to de-instrument any code that has 'gone cold' (col. 29, lines 21-24 'target address of a translated instruction ... is replaced with the address ... in original instruction storage').

**Regarding Claims 5, 10 and 15:** The rejections of claims 4, 9 and 14 are incorporated respectively; further Benitez discloses comparing said return addresses of said process to said address in said instrumented code space which generated said fault upon execution of said process (col. 27, lines 63-67 'backpacker searches hot block-arc table to determine if any ... block has a jump instruction that jumps to the block from which translated instructions were translated').

#### *Response to Arguments*

**8. Applicant's arguments in last paragraph of pg. 5 of the remarks filed 2/23/05 have been fully considered but they are not persuasive.**

In the last paragraph on pg. 5, Applicant states:

Benitez does not teach a process let alone "...reverting a process in an in-line instrumented state to an uninstrumented state," as recited by Claim 1. Instead, as already discussed herein, Benitez discloses determining the frequency with which traces are executed.

Examiner Respectfully disagrees. 'A process' as known in the art is simply an executing program, which Benitez clearly discloses (Abstract 'an executable file at run time').

Further while Benitez does disclose 'determining the frequency with which traces are executed', it is Examiner's position, for the reasons of record and those discussed below, that Benitez also discloses the limitations claimed in the instant application.

**9. Applicant's arguments in first paragraph of pg. 6 of the remarks filed 2/23/05 have been fully considered but they are not persuasive.**

In the first paragraph on pg. 6 Applicant states:

The rejection states that "unmapping instrumented code space such that said instrumented code space is inaccessible to said process," as recited by Claim 1 is disclosed by Benitez at Col. 27, lines 49-51. Although Benitez at Col. 27, lines 49-51 discloses "backpatching a jump or fall-through instruction...", this portion of Benitez (e.g. Benitez at Col. 27, lines 49-51) does not disclose "unmapping" anything let alone "unmapping instrumented code space such that said instrumented code space is inaccessible to said process.

Examiner respectfully disagrees. First, the text cited by Applicant is not the text referenced by Examiner in his action, but instead can be found at col. 29, lines 15-16. However, in addition to the reasoning put forth in the rejections, if we read on we find that Benitez discloses 'backpatcher backpatches a jump or fall-through instruction so that a target address of a translated instruction ... is replaced with the address of the corresponding original instruction', thereby 'unmapping' instrumented code space.

**10. Applicant's arguments in the last paragraph on pg. 6 with respect to claims 1, 6 and 11 have been considered but are moot in view of the new ground(s) of rejection.**

In the last paragraph on pg. 6, Applicant states:

The rejection states that "executing said process and, provided said process generates a fault by seeking to access an address in instrumented code space, providing a corresponding address in said uninstrumented code space," is disclosed by Benitez at Col. 11, lines 28-38. However, this portion of Benitez (e.g., Col. 11, lines 28-38) does not even disclose executing a process. Instead, this portion of Benitez (e.g., Col. 11, lines 28-38) discloses terminating the operation of a trace designator 100. Further, Benitez does not teach providing a corresponding address in said uninstrumented code space as the result of a fault generated by the execution of a process. In order for Benitez to teach ... Claim 1, Benitez would have to teach among other things, that a process generates a fault by seeking to access an address of Benitez' "original code"

Respectfully, Benitez' "trace designator" dynamically evaluates a control path (col. 9, 37-39), inherently disclosing execution of a process. Further it is Benitez' "hot traces" which contain the instrumented code (col. 9, lines 62-65 'instruments such translated hot traces'), and not his "original code", therefore Benitez discloses providing an address in uninstrumented code space. However, upon further consideration, and as addressed above, it has been found that Benitez does not explicitly disclose that this address is provided in response to a fault generated by seeking to access an address in instrumented code space.

**11. Applicant's arguments with respect to claims 2-5, 7-10 and 12-15 have been considered but are moot in view of the new ground(s) of rejection.**

Applicant's arguments regarding these claims rely on the patentability of claims 1, 6 and 11. As claims 1, 6 and 11 have been addressed with a new rejection, Applicant's arguments regarding claims 2-5, 7-10 and 12-15 are now moot in view of this new rejection.

In the first paragraph on pg. 8, Applicant states:

Therefore, the rejection cited in paragraph 8 should be a 102 rejection since the primary and the secondary reference are the same reference.

It is Examiner's understanding that because certain limitations of the instant claims are not explicitly taught by Benitez, but are obvious over Benitez's teachings the rejection under U.S.C. 103(a) is proper.

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Mitchell whose telephone number is (571) 272-3728. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kakali Chaki can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

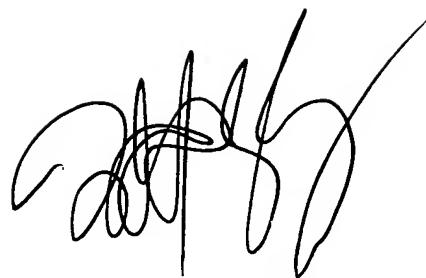
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Art Unit: 2193

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Jason Mitchell  
5/11/05



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PRIMARY EXAMINER**